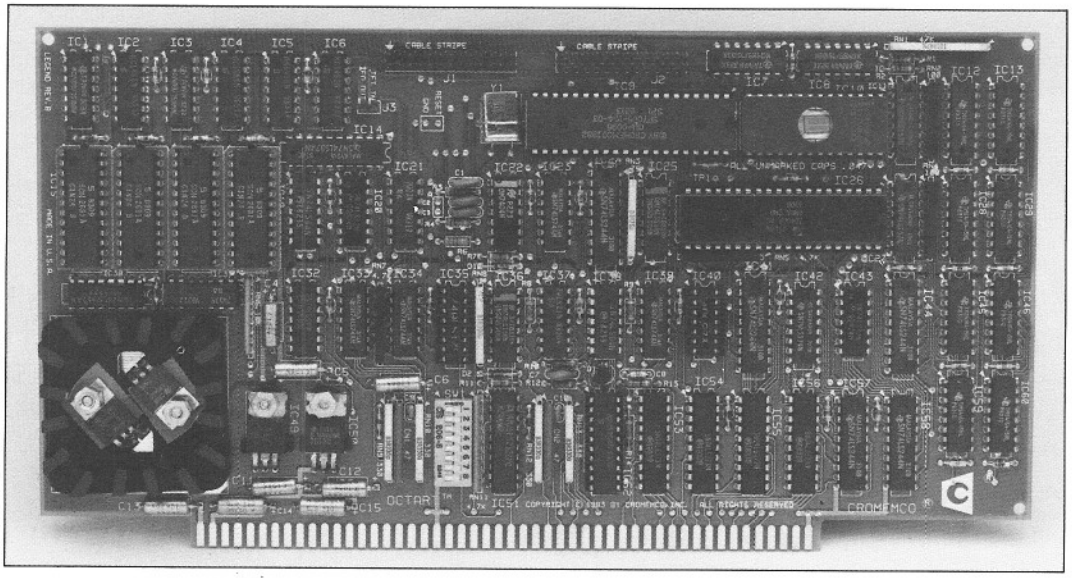
MODEL OCTRT
OCTART 8-Channel Asynchronous Serial Interface



FEATURES

- ☐ Intelligent single board communications controller using Z80A with 16KB of ROM and 64KB of RAM
- ☐ Eight independent serial channels with handshake
- ☐ Asynchronous, high speed communications to 38.4K baud, with provision for user defined baud rate to 125K baud
- ☐ Transmit and receive baud rates set independently
- ☐ Four multifunction programmable 16-bit counter-timers
- ☐ Download of driver and/or application software to run on the board relieving the host system.

The OCTART is an intelligent communications controller serving as a slave processor on the S100 (IEEE 696) bus. It is an economical way to add high speed asynchronous communications.

Eight independent serial channels provide flexibility in selecting the mode of asynchronous communications: Data length can be selected from 5 to 8 bits; parity mode may be chosen in odd, even, none or forced high or low; stop bit length may be varied from 1 or 2 bits in increments of 1/16 bit; baud rate may be chosen from 18 values between 50 to 38.4K baud. Four 16-bit counter-timers are also available.

The OCTART supports full duplex, auto echo and local and remote loopback on each channel. Each channel also has transmit data, receive data, request to send, clear to send and ground signals.

The software program in ROM allows you to download your own device drivers or application programs into RAM. The ROM is then mapped out leaving the full address space of the Z80A.

Terminal Support software is provided in the Cromix and UNIX System V operating systems.

TECHNICAL SPECIFICATIONS

Processor: Z80A

Clock Rate: 3.6864MHz

Memory: 16KB EPROM/ROM, may be bank selected in or out under program control

64KB RAM, upper and lower 16KB sections alternate with ROM memory through program controlled bank select

Interrupts: On-card interrupts for character handling, break detection, counter/timer ready, and host data transfer

S-100 interrupts for OCTART data transfer
Programmable 8-bit interrupt vector
Supports daisy-chain priority system

Reset Modes: Reset via main bus reset line or by software command from host

Serial Channels: Eight independent serial channels implemented with four 2681 chips

Parity modes: odd, even, none or force. False start bit detection, line break detection and generation

Serial Protocols: Asynchronous

Serial Rates: 50 to 38,400 baud asynchronous

RS-232 Signal Support: RTS, CTS, TxD, RxD and GND

Counter Timing: Four 16-bit counter-timers

Bus: S-100

Power Requirements: + 8 volts @ 1.5A
± 16 volts @ 100 mA

Operating Environment: 0–55 degrees Centigrade

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